2.3 A 3MPixel Multi-Aperture Image Sensor with 0.7μm Pixels in 0.11μm CMOS

Keith Fife, Abbas El Gamal, H.-S. Philip Wong

Stanford University, Stanford, CA

Conventional image sensors have improved with technology scaling mainly by reducing pixel size to increase spatial resolution [1,2]. As resolution approaches the limits of existing optics, is there much to gain from further pixel scaling? In [3], we argue that further scaling can provide new imaging capabilities via a multi-aperture (MA) architecture, which consists of an array of small submicron pixel imagers (apertures), each with its own integrated optics. By focusing the integrated optics onto an image plane formed by an objective lens in a region above the MA imager, the apertures capture overlapping views of the scene. The correlation and redundancy between apertures, along with computation, provide several new capabilities, including: (i) simultaneous capture of a 2D image at higher resolution than the aperture count and a 3D depth map without the need for active illumination or calibration; (ii) simplification of the objective lens design; (iii) reduction of color crosstalk via per-aperture color filters; and (iv) increased tolerance to pixel defects. It is further shown that depth resolution continues to improve with pixel scaling beyond the typical spot-size of the optics. Designing scalable arrays of submicron pixels with acceptable imaging performance is challenging however. In [3], we propose using a frame-transfer (FT) CCD aperture with CMOS readout architecture. In [4], we demonstrate a 16×16, 0.5μm pixel-pitch FT-CCD in 0.11μm CMOS technology with acceptable imaging performance.

In this paper we describe the first complete MA-imager chip comprising a 166×76 array of 16×16, 0.7μm pixel FT-CCD apertures, per-column ADCs, control logic and chip readout circuits fabricated in 0.11μm CMOS technology[1]. Figure 2.3.1 shows a block diagram of the MA-imager. The aperture control buses, V<35:0> and H<15:0> are globally connected to the FT-CCDs. The RS signal and the decoded ROW bus are used to address the readout circuits for each row of FT-CCDs. The MUX blocks contain column bias circuitry, inputs for external testing of the ADC and support for analog pixel readout through AOUT. The ADCs share an output bus that is decoded by COL and buffered for digital readout through DOUT<10:0>.

Figure 2.3.2 shows a schematic of the FT-CCD, which consists of a pixel array free from metal layers, a light shielded frame buffer, a horizontal (H) CCD with floating diffusion (FD) and follower readout circuit. The CCDs are formed using P+ poly electrodes over N-type channel implants with P+ channel stops. The inputs to the channels at the top of the array are connected to V0 through an Nwell implant. The P+ channel stops extend beyond the Nwell region to make an effective contact to the substrate potential. The two sides of the H-CCD connect to VP, which is used for fill/spill operation, reset of the FD node, or as the source-follower drain supply. Charge is collected under every other electrode, which facilitates large potential barriers between pixels. An STI (Shallow Trench Isolation) region is used to create isolation between apertures and as the area for contacts to the non-silicided electrodes.

The chip operation is divided into three phases: FLUSH, INTEGRATE, and TRANSFER (see Fig. 2.3.3). Each frame consists of 2 interlaced fields. The capture of one field is performed at the same time as a previous field is being read out from the frame buffers. During FLUSH, the CCD pixel arrays are depleted of charge through V0 by sequencing V<17:1>. During integration, the pixel array electrodes are held at an intermediate voltage of 1V. At the end of integration, the accumulated charge packets in

the CCD pixel arrays are transferred one row at a time to the frame buffers using ripple charge transfer. A 2V potential difference between electrodes is used to achieve complete transfer between stages. Frame buffer readout is performed while a new INTEGRATION cycle takes place after a FLUSH cycle. The readout sequence begins with a global reset of all FD nodes through an RT pulse. The reset voltages are then digitized by the per-column ADCs one aperture row at a time and stored off chip. Next, one charge packet from each frame buffer is shifted to its H-CCD (see Fig. 2.3.3), which is performed by initially shifting one row of charge to the V35 electrode. One of the horizontal electrodes, e.g., H15, is set to a high voltage, which causes a partial charge transfer. Next, V34 is brought to an intermediate voltage while V35 is slowly brought to a lower voltage. The charge is transferred to H15 because the fringing field induced by H15 is larger than that induced by V34. This completes the transfer for the desired charge packet while all other charge is moved back under V34. The charge in the H-CCD is then ripple shifted to H0 and onto the FD node while pulsing TX high. The pixel values on the FD nodes are digitized one row at a time by the ADCs and stored off chip where digital CDS is performed. This sequence is repeated until all stored pixel values for one field are read out. This readout approach eliminates the need to implement a row decoder for each of the frame buffer and H-CCD electrodes.

Figure 2.3.4 shows the per-column ADC schematic and timing diagram. A single-slope architecture with off-chip ramp (via a 14b DAC) is used for flexible operation. Conversion begins by resetting the keeper. As the COLUMN voltage settles, SAMPLE is continuously clocked while the bus signal C is cycled through gray code values corresponding to levels of the RAMP voltage. We exploit the fact that shot noise power increases with the signal to reduce conversion time by increasing the step size of the RAMP over the signal range. Once RAMP exceeds COLUMN, the code on C is latched into buffer A. The keeper stays latched until the beginning of the next conversion where buffer B is used to store C while buffer A is read out. Programmable column gain is achieved by varying the ramp voltage range from 200mV to 2V. The comparator consists of a diff-pair followed by a regenerative latch. The diff-pair transistors have a W/L ratio of 6 to keep them in weak inversion. With a 1μA bias current, the comparator is capable of 10b resolution at 200MSPS over a 200mV range. The regenerative portion of the comparator and the memory buffers are implemented with 1V transistors, while the diff-pair is implemented with 3V transistors, allowing for simple translation between power domains.

A chip micrograph is shown in Fig. 2.3.5. The chip characteristics and image sensor performance are listed in Fig. 2.3.6. Figure 2.3.7 shows a sample image at full resolution captured with a fixed focus F/2.4 lens in a standard focal plane imaging configuration. Note that the images captured by the individual apertures demonstrate measurable detail.

References:
[1] M. Oda, T. Kaida, S. Izawa et al., "A 1/4.5in 3.1M Pixel FT-CCD with 1.56μm Pixel Size for Mobile Applications," *ISSCC Dig. Tech. Papers*, pp. 346-347, Feb. 2005.
[2] G. Agranov, R. Mauritzson, S. Barna, et al., "Super Small, Sub 2μm Pixels for Novel CMOS Image Sensors," *2007 International Image Sensor Workshop*, pp. 307-310, June 2007.
[3] K. Fife, A. El Gamal and H.-S. P. Wong, "A 3D Multi-Aperture Image Sensor Architecture," *Proc. CICC*, pp. 281-284, Sep. 2006.
[4] K. Fife, A. El Gamal and H.-S. P. Wong, "A 0.5μm Pixel Frame-Transfer CCD Image Sensor in 110nm CMOS," *IEDM Tech. Dig.*, pp. 1003-1006, Dec. 2007.

[1]Local optics are not integrated on this chip.

978-1-4244-2011-7/08/$25.00 ©2008 IEEE

Please click on paper title to view a Visual Supplement.

2
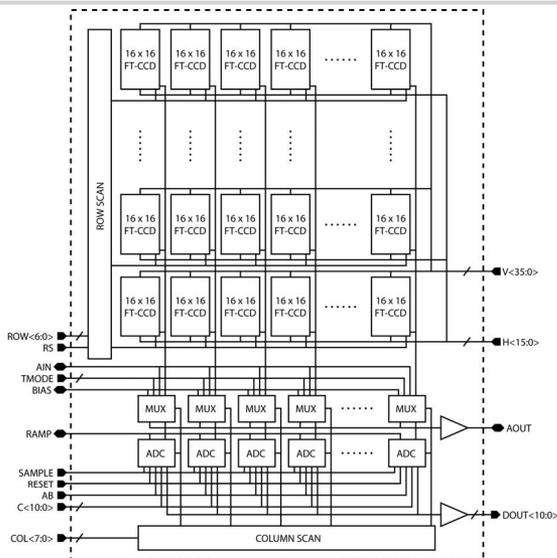
Figure 2.3.1: Block diagram of MA image sensor chip.
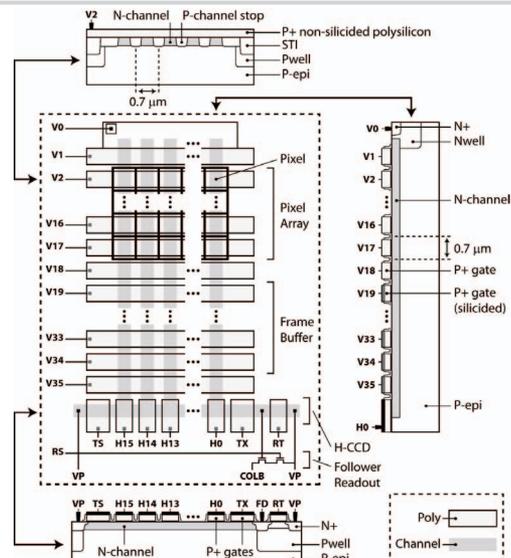
Figure 2.3.2: FT-CCD schematic and device cross sections.
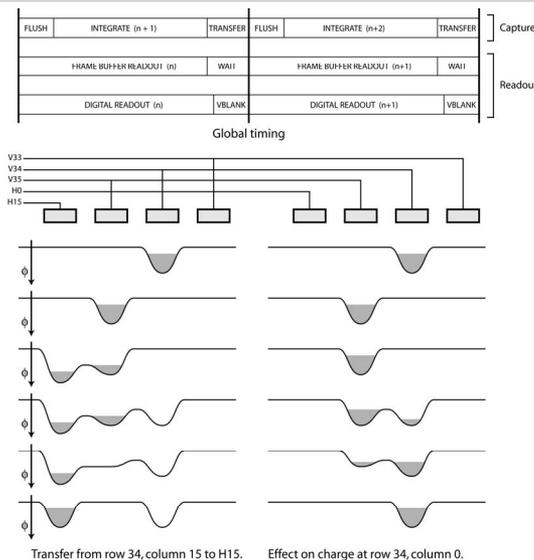
Figure 2.3.3: Chip timing and charge transfer diagram.
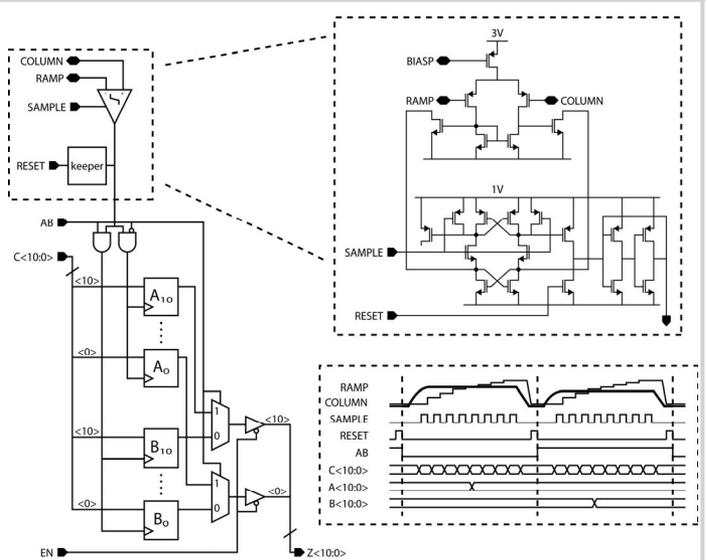
Figure 2.3.4: Per-column ADC schematic and timing diagram.

Figure 2.3.5: Chip micrograph.

Technology	0.11μm 1P4M CMOS CIS
Chip Size	3.0 x 2.9mm²
Aperture count	166 x 76
Aperture format	16 x 16 pixels
Pixel size	0.7μm x 0.7μm
Well capacity	3500 e-
Conversion gain	165 μV/e-
Sensitivity at 550 nm	930 e-/lux-sec (0.15V/lux-sec)
QE at 450, 550, 650 nm	20, 48, 65 %
Pixel read noise	5 e- rms (1mV)
Dark current at room temperature	33 e-/sec (5.5 mV/sec)
Intra aperture DSNU	35 % rms
Inter aperture DSNU	4 % rms
Intra aperture PRNU	2 % rms
Inter aperture PRNU	2 % rms
Peak SNR	35 dB
Dynamic range	57 dB
Maximum Frame rate with CDS	15fps
ADC resolution	10b
ADC FPN	43μV rms
ADC noise	254 μV rms
ADC INL/DNL	(0.46,-0.60)/(0.39,-0.57) LSB
Chip power	10.45mW

Figure 2.3.6: Chip characteristics and imager performance at 7.5 fps.

Please click on paper title to view a Visual Supplement.

ISSCC 2008 PAPER CONTINUATIONS
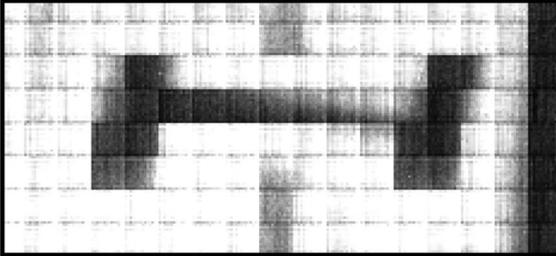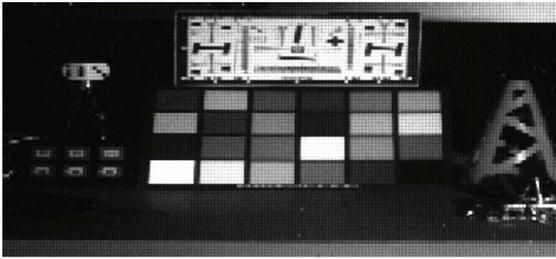
Figure 2.3.7: Sample image at full resolution (top) with detailed section (bottom).